REMARKS

In the Drawings

Formal drawings are submitted with this response. The drawings have not been amended.

In the Claims

Claims 27-47 have been rejected under 35 USC 103(a) as being unpatentable over U.S. patent no. 4,611,236 ("Sato") in view of U.S. patent no. 5,780,883 ("Tran"). Applicant respectfully traverses this rejection because the cited references do not disclose or suggest every limitation of any pending claim, as the following analysis shows. In particular, the cited references only show that different size transistors exist, and that internal clock buffers exist, but the rejection has failed to address the specific limitation of using smaller transistors as internal clock buffers.

Independent claims 27 and 38 recite that the smaller transistors are used to form internal clock buffers. Contrary to the statements in the rejection, Sato does not disclose or suggest this limitation. Sato never mentions clocks, either internal or otherwise, in any context. Sato only mentions buffers in general, and teaches away from the claimed limitations by stating that higher capacity (i.e., larger) transistors are to be used for buffers (col. 3 line 26). On page 2 of the Office action, the rejection states that Sato "discloses in figure 8 that the transistors can be used to form the internal clock buffer; it is well known that the internal clock buffer comprises two inverters." In fact, figure 8 only discloses a series of inverters, but never describes what the inverters might be used for.

It requires impermissible hindsight to make an unsubstantiated statement of what might be well known and use that as proof of obviousness. Section 2143 of the Manual of Patent Examining Procedure ("MPEP") sets forth the requirements that must be

satisfied to establish a prima facie case of obviousness under 35 USC 103. Section 2143 requires the cited references to contain a suggestion or motivation to combine them. The rejection fails to make this showing because it does not point out a suggestion or motivation to combine from within the references. Instead, it only makes a conclusory statement of what is well known, without any indication of what teaching in the references would show what was well known. This reasoning engages in hindsight speculation that section 2143 and the Federal Circuit expressly proscribe: "the level of skill in the art cannot be relied upon to provide the suggestion to combine references," (MPEP 2143, citing *Al-Site Corp. v. VSI Int'l Inc.*, 174 F.3d 1308 (Fed. Cir. 1999)).

It is noteworthy that section 2143 takes pains to make this point clear, elaborating that "a statement that modifications of the prior art to meet the claimed invention would have been 'well within the ordinary skill of the art at the time the claimed invention was made' because the references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish a prima facie case of obviousness with some objective reason to combine the teachings of the references." (citing *Ex parte Levengood*, 28 USPQ2d 1300, Bd. Pat. App. & Inter. 1993). By repeating the mistakes criticized in section 2143 and failing to show a suggestion or motivation to combine the cited references, the rejection has failed to establish a prima facie case of obviousness under 35 USC 103.

Although Tran was not cited in connection with this limitation, Tran also does not mention clocks in any context, and only describes buffers as requiring larger transistors (col. 3 lines 15-17).

The role of Faue in this rejection is not clear. Page 3 of the Office action states that Faue teaches that two inverters can be used to form an internal clock buffer, citing col. 3 lines 4-5. However, Faue was never cited as a reference in the statement of

rejection. Since Faue was not cited as prior art, this reasoning can only be interpreted as trying to use an uncited reference to illustrate what is known, and then using what is indicated as known to show motivation to combine the cited references. As described above, this line of reasoning is prohibited by both the MPEP and the applicable case law. If Faue is to play any part in the rejection, Faue should be cited as a prior art reference in the statement of rejection. However, even if a future rejection were to cite Faue as prior art, Faue still does not show the use of smaller transistors as internal clock buffers.

In the last sentence of the first paragraph of page 3 of the Office action, the Examiner states "Applicant failed to provide evidence to show that the two inverters connected in series as disclosed by Sato are not internal clock buffer." This statement reverses the legally-mandated burden of proof in examination of a patent application. Under the applicable statutes, rules, and sections of the MPEP, the Applicant's claims are presumed allowable until shown to be not allowable by the Examiner. The Examiner has failed to provide this showing, and instead has stated that the Applicant has failed to provide a burden of proof which the Applicant has no obligation to provide.

The remaining pending claims depend from claims 27 and 38, and therefore contain the same limitations that are not disclosed or suggested by the cited references.

In summary, none of the references disclose or suggest the use of smaller transistors as internal clock buffers. Two of the references (Sato, Tran) specifically teach against this practice, while a third reference (Faue), which was referenced but never cited, never mentions the use of different sizes of transistors for any purpose. The cited references only show that different size transistors exist, and that internal clock buffers exist, but has failed to address the specific limitation of using smaller transistors as internal clock buffers.

CONCLUSION

For the foregoing reasons, Applicants submit that the application is now in condition for allowance, and indication of allowance by the Examiner is respectfully requested. If the Examiner has any questions concerning this application, he or she is requested to telephone the undersigned at the telephone number shown below as soon as possible. If any fee insufficiency or overpayment is found, please charge any insufficiency or credit any overpayment to Deposit Account No. 02-2666.

Respectfully submitted,

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John Travis
Intel Corporation
Reg. No. 43,203

Correspondence address:

Blakely Sokoloff Taylor & Zafman LLP
12400 Wilshire Blvd
Seventh Floor
Los Angeles, California 90025-1026

Attorney phone:

(512) 314-0334

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